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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/005,135 | 11/30/2001 | Phillip M. Adams | 2456.2.9 | 8062 |

7590 11/17/2003

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| EXAMINER | |
|---|---|
| CHEN, ALAN S | |
| **ART UNIT** | **PAPER NUMBER** |
| 2182 | 5 |

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/005,135 | ADAMS, PHILLIP M. | |
| | Examiner | Art Unit | |
| | Alan S Chen | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-14 and 16-24* is/are rejected.

7)☒ Claim(s) *3 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 66 of Fig. 2, 136 of Fig 8 and 170 of Fig. 10. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1,4,13 and 22-24 rejected under 35 U.S.C. 102(b) as being anticipated by No. 4,996,690 to George et al. (hereafter George).

In reference to claim 1, 22 and 24, George discloses an apparatus and article (Fig. 1) for correcting errors in data transfer undetected by the transferring hardware devices of both synchronous (Fig. 1, element 12) and asynchronous (Fig. 1, elements 10 and 12) types, the apparatus comprising:

A processor (Fig. 1, element 10) that can process data from synchronous and asynchronous types; and

A controller configured to control data exchange between devices (Fig. 1, element 14), the controller including a buffer (Fig. 1, element 22 and 24).

A memory device connected to the processor to store data structures comprising executables (Fig. 2, element 70), the executables comprising:

A driver configured to control operation of the controller (Fig. 2, element 66 sends control signals to Buffer Manager, Fig. 1, element 22).

An error avoidance module (Fig. 2, element 72) configured to be invoked by the driver to compare the capacity to a count of bytes (see "count" method in Fig. 6), and force an error condition based on count (via the gating means, see Abstract).

In reference to claim 4, George discloses the apparatus of claim 1, wherein the driver further comprises an initialization module configured to enable the error avoidance module (Column 6, lines 15-45).

In reference to claim 13, George discloses an apparatus (Fig. 1) for correcting errors in a computer system configured to communicate with devices of both synchronous and asynchronous types, the method comprising:

Transferring bytes of data between a device (Fig. 1, element 12) and a buffer having a capacity (Fig. 1, element 24);

Providing a count of the bytes (Fig. 2, element 72);

Comparing the count to the capacity (see "count" method in Fig. 6); and

Forcing an error condition based on the count (via the gating means, see Abstract).

In reference to claim 23, George discloses the article of claim 22, wherein the driver further comprises an initialization module configured to enable the error avoidance module (Column 6, lines 15-45).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 14 are rejected under 35 USC 103(a) as being unpatentable over George in view of No. 6,151,180 to Bang.

George discloses the apparatus of claim 1 and 13.

George does not disclose expressly the error condition being forced if the value of the count is as large as the capacity.

Bang discloses an apparatus where the error condition (performing the error correction code) is forced if the value of the count is within the capability of the Error Correction Code (Column 4, lines 39-59).

Bang and George are analogous art because they are from the same field of endeavor in detection and correction of errors in disk drives.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify George's invention to define a condition for when the error condition to occur within the capability the error correction code.

The suggestion/motivation for doing so would have been to maximize the correction of defects while identifying the defects that could not be corrected (Column 1, lines 44-57).

Therefore, it would have been obvious to combine George with Bang for the benefit of forcing the error condition based on the capability of the ECC.

6. Claims 5-10, 16-19 and 20 are rejected under 35 USC 103(a) as being unpatentable over George in view of No. 4,189,765 to Kotalik et al. (hereafter Kotalik).

George discloses the apparatus and method of claims 1 and 13, wherein the driver further comprises an initialization module configured to enable the error avoidance module (Column 6, lines 15-45), in addition to the module detecting a write operation.

George does not disclose expressly a limit, a plurality of limits, or high/low limits of the buffer for when to enable an interrupt.

Kotalik discloses an apparatus and method (Fig. 4) wherein an upper limit and lower limit is able to be established for which a control signal must fall between (Column 3, lines 28-36). Furthermore, an alarm is triggered when deviations from the limit are realized. This alarm is an audible alarm, and serves as an error avoidance module (Column 4).

Kotalik and George are analogous art because they are from the same field of endeavor in error detection.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify George's invention to include a high and low limit similar to Kotalik's, upon which the error avoidance module is triggered when a one of the limits are surpassed.

The suggestion/motivation for doing so would have been to give a margin of operation for the buffer specified by George to operate before action is taken in error avoidance (Column 4, lines 41-60).

Therefore, it would have been obvious to combine Kotalik with George for the benefit of setting boundary conditions for operation of the buffer and executing error avoidance module when the boundary is crossed.

7. Claims 11, 12 and 21 are rejected under 35 USC 103(a) as being unpatentable over George in view of Kotalik in further view of Bang.

George discloses the apparatus and method of claim 1 and 13. Kotalik discloses the apparatus and method of claims 9 and 20.

Both do not disclose expressly the error avoidance module configured to detect both a read and a write operation. Nor do both disclose expressly the buffer consisting a register, FIFO, and content-addressable memory.

Bang discloses an error avoidance module configured to detect both a read and write operation (Fig. 3, element 212) and the buffer being a FIFO (Fig. 3, element 256) selected from the group consisting a register (Fig. 3, element 266), a FIFO (Fig. 3, element 256) and an addressable memory (Fig. 3, element 270).

George, Kotalik, and Bang are analogous art because they are from the same field of endeavor in error detection.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Kotalik's invention to detect both read and write operations since errors can occur in either operations. Further, the selection of the buffer is a design choice and the FIFOs are very well known and widely used in the art.

The suggestion/motivation for doing so would have been to detect errors in both read and write operations since errors described by applicant can occur whenever data is transferred from one location to another.

Therefore, it would have been obvious to combine George, Kotalik and Bang for the benefit of detecting both a read and write operation and using a FIFO as the buffer.

***Allowable Subject Matter***

8. Claims 3 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, an apparatus or method as stated in claim 1 and 13, wherein the error condition is forced if the value of the count is at least as large as the capacity of the buffer added to a value corresponding to bytes that have been transferred both into and out of the buffer during a transfer operation between the buffer and a processor.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to error correction in I/O systems:

U.S. Pat. No. 4,206,440 to Doi et al.

U.S. Pat. No. 4,216,532 to Garetti et al.

U.S. Pat. No. 5,267,241 to Kowal

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

asc
9/15/2003